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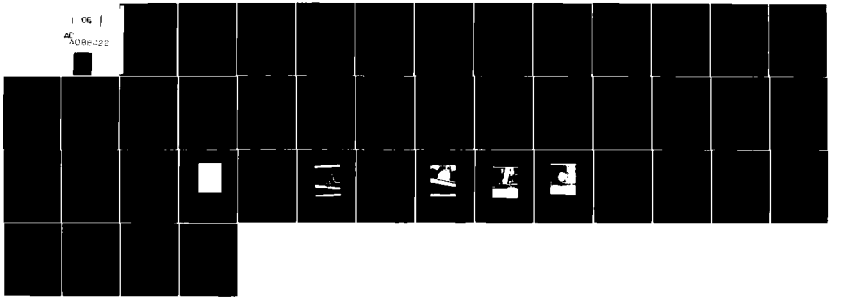

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SUBMICRON FETs USING MOLECULAR BEAM EPITAXY

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Electron-beam exposure and MBE material have been used to achieve quarter-micron gate length GaAs FETs. A noise figure of 1.5 dB with an associated gain of 15 dB has been measured at 8 GHz.

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FOREWARD

The work reported here was supported by the Office of Naval Research, Washington, D.C., under contract N00014-77-C-0655, and managed by Mr. Max Yoder. The program was aimed at developing FETs with gate lengths of around 0.25 micron and looking for any evidences of velocity overshoot.

The work was carried out in the Varian Corporate Research Solid State Laboratory. The authors wish to thank M. Pustorino, S. Lombardi, and J. Dully for technical assistance and G. Antypas for providing the GaAs substrate material. The Varian Vacuum Division is gratefully acknowledged for providing the MBE-360 system used in this work. Valuable discussions with M. Yoder and R. L. Bell are gratefully acknowledged.

SUMMARY

Using electron-beam exposure and MBE GaAs, FETs have been fabricated with gate lengths ranging from 0.16 to 0.25 micron. A noise figure of 1.5 dB with an associated gain of 15 dB has been measured at 8 GHz. Problems with gate and source resistance appear to be limiting the performance. Steps have been taken to remedy the high gate resistance by going to a new FET geometry, with the full benefits of this geometry yet to be realized.

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1. INTRODUCTION

The Introduction to Annual Report No. 1 will be repeated here, followed by a brief summary of the accomplishments during that period and the problem areas to be dealt with as perceived at the start of this reporting period.

"Transient velocity overshoot" was proposed by Ruch[1] in 1972 to explain why GaAs, while having only a marginal advantage over Si with regard to the saturated drift velocity in the high field region (Fig. 1), is able to outperform Si in a FET structure. Cold electrons injected at the source may never reach their steady-state velocity before being collected at the drain, but travel at a higher velocity, approximately

$$v = \mu_o E \qquad (1)$$

where μ_o is the low field mobility, before relaxation effects take place. This transient phenomenon is due to the disparity between the energy and momentum relaxation times, causing the average velocity in the channel to overshoot its usual saturation value.

Figure 2 shows a computed plot of velocity vs. distance down the channel for both GaAs and InP, assuming a constant field.[2] These plots illustrate the significant role that velocity overshoot can play in increasing the effective electron velocity in submicron gate devices. Silicon also shows velocity overshoot, but the improvement is much smaller and would require gate lengths less than 1000 Å to realize it.[1] It may thus be possible to increase the

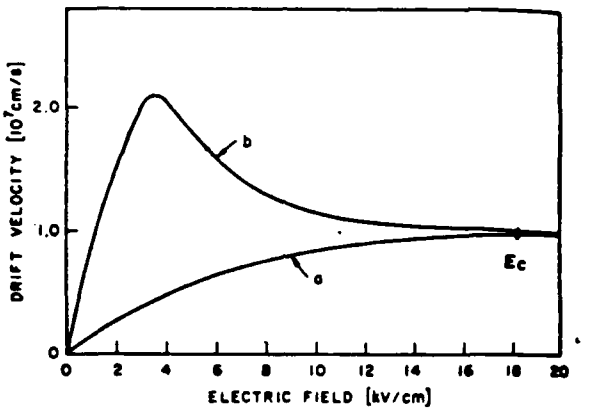


Fig. 1. Velocity-field characteristics in GaAs and silicon.[1]

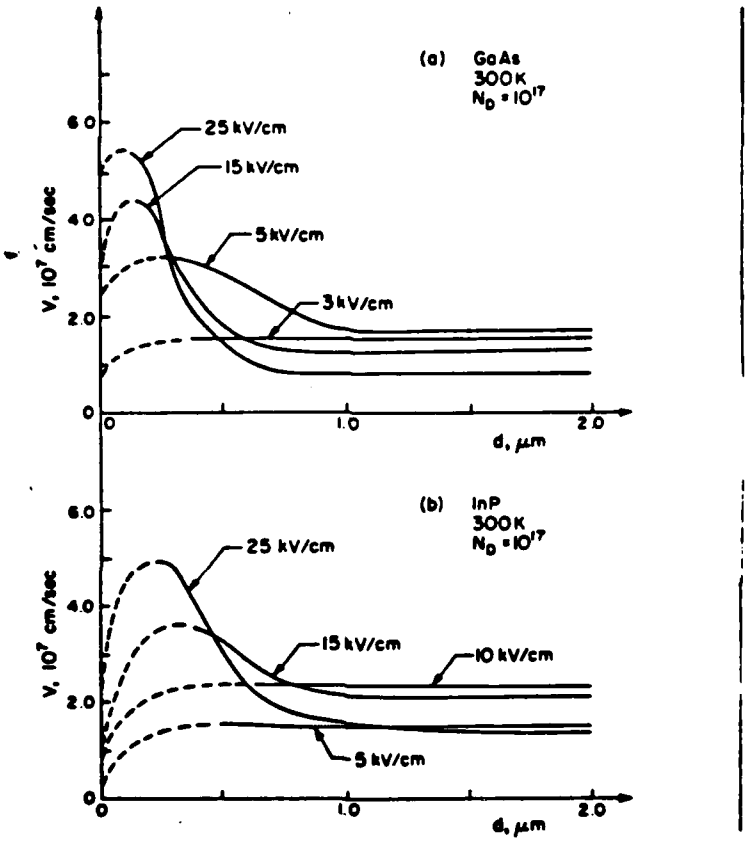


Fig. 2. Instantaneous velocity vs distance for 300°K, $N_a = 10^{17}$, (a) GaAs, (b) InP.[2)]

effective saturated velocity in the FET channel without resorting to "super velocity" materials, by reducing the gate length to GaAs FETs.

It may well be that the proposed performance advantages of "super velocity" alloys such as InGaAsP will only be realized by the mechanism of velocity overshoot. As shown by the computations of Littlejohn, et al.[3] in Fig. 3, while the computed static velocity-field characteristic of InGaAsP shows a higher low field mobility, which can be utilized by velocity overshoot according to Eq. (1), the velocity in the high field region is less than that of GaAs. Thus, the investigation of the transient effects of velocity overshoot for other materials such as InP, InGaAs, InGaAsP and other promising materials is also a matter of importance.

In addition to the benefits available from higher carrier velocities in the channel, FET performance is, of course, improved directly by scaling down dimensions. However, besides the ability to provide quarter-micron openings in resist with electron beam photolithography, the gate metallization scheme must preserve the resist profile, the active layer must be thinner to prevent g_m reduction, and the effective source-gate spacing must be reduced to avoid source resistance domination. In addition to all this, it may be that a reduction in device width or the addition of multiple gate pads may be necessary to overcome the increased gate resistance brought about by using such small gate lengths. If a narrower-width device is used, it may be necessary to integrate a driver FET of larger dimensions on the same ship to drive the off-the-chip-parasitics involved in the reali-

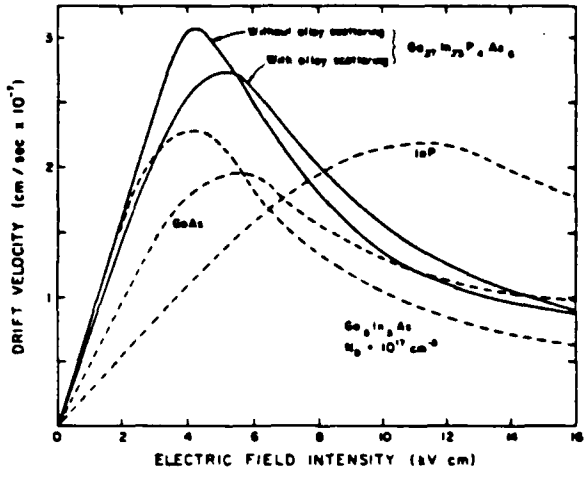


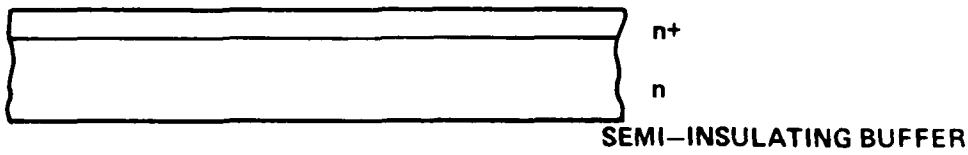
Fig. 3. Velocity-field characteristic of $Ga_{0.27}In_{0.73}P_{0.4}As_{0.6}$ with and without random potential alloy scattering. Shown for comparison are the velocity-field curves for GaAs, InP, and $Ga_{0.5}In_{0.5}As$. The doping level is $10^{17}cm^{-3}$.3)

zation of practical broadband microwave amplifiers (being a second stage, its gain and noise figures are of less importance).

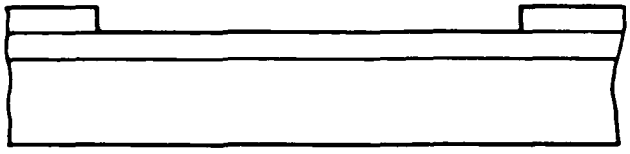
Concerning the progress made during the first period, GaAs FETs were fabricated on MBE material using an anodic thinning procedure to remove the n^+ layer in the immediate vicinity of the gate (Fig. 4). The gates were defined by electron-beam exposure and ranged in length from 0.15 to 0.45 micron. The use of the n^+ layer resulted in very low source resistance (3.1 ohms) and very high g_ms (30-32 mmhos). The best rf data obtained at 8 GHz was a minimum noise figure of 2.2 dB with an associated gain of 12 dB for devices with gate lengths ranging from 0.3 to 0.45 micron.

In terms of device performance, it appeared that gate resistance was a limiting factor in the noise performance. In terms of yield, anodization damage to the ohmic contacts still occurred even with the use of Ti-W to promote adhesion of the oxide to the ohmic contacts. Another problem area was the uncertainty in the exact doping profile of the MBE wafers, making it difficult to determine, with sufficient accuracy, how much GaAs should be anodically thinned off in the gate region. Profiling is difficult because of the high doping of the n^+ layer and the leakage encountered by the Schottky-barrier dots on the lower-doped active layer, a difficulty common to early MBE materials. These problem areas formed the basis of immediate concern on the current phase of the contract.

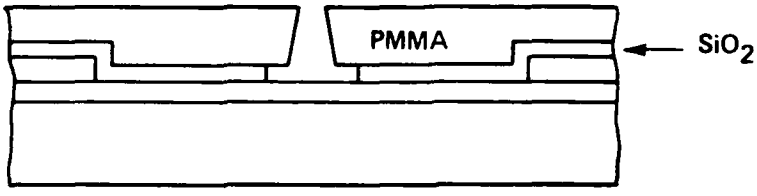
Once a device structure exists which is free enough from the effects of parasitics and other degradation pheno-



(a) STARTING MATERIAL



(b) OHMIC CONTACTS



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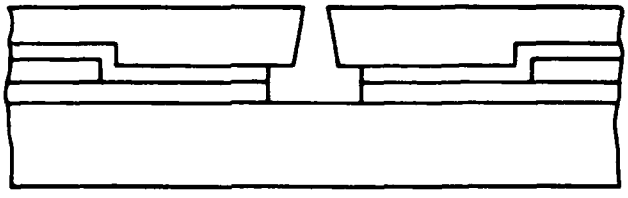
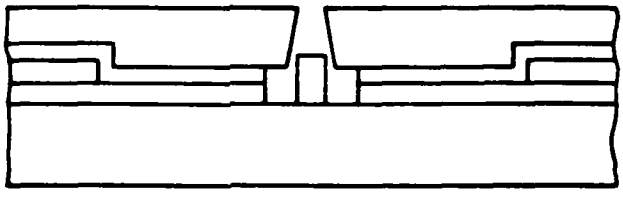


(d) ANODIC ETCH



(e) GATE DEPOSITION

Fig. 4 Gate anodization process.

mena to allow study of the properties of the intrinsic device, the ultimate goals of this contract can be addressed:

(1) Determination of the optimum channel thickness and doping for a given gate length.

(2) Fabrication on different crystalline orientations to observe any anisotropy of the electron velocity overshoot effect that may occur. This will be done by determining the effective saturated drift velocity, v_s, by the techniques developed under ONR Contract N00014-77-C-0125[4] and described in the final report of that contract.

(3) Evaluation of the use of an MBE AlGaAs buffer layer for carrier confinement to the active layer.

2. BRIEF OVERVIEW OF PROGRESS

Table I gives a compilation of the device results obtained during this period. Section 3 describes in more detail the problems and the evolution of technology with the progression of the device runs. Section 4 outlines the steps taken to reduce the gate resistance.

The minimum noise figure, $NF_{m\ calc}$ is computed from the BTL formula[5]

$$NF_m = 1 + KfL^{5/6}\left(\frac{N_D}{a}\right)^{1/6} Z^{1/2}\ (r_c + r_g + R_s)^{1/2} \quad (2)$$

where K = 0.033 for "good" FETs, f is the frequency in GHz, L is the gate length in microns, N_D is the channel doping in units of $10^{16}cm^{-3}$, a is the active layer thickness in microns, and Z is the gate width in mm. r_c is the intrinsic channel resistance and r_g and R_s are the parasitic gate and source resistances, respectively.

Whereas the best results obtained in the previous period were NF_m = 2.2 dB, G_a = 12.2 dB for Run EB6, Table I shows a significant improvement in this result to NF_m = 1.5 dB, G_a = 15 dB brought about mainly by a reduction in L (the 2.2 dB for Run EB6 was for L = 0.3-0.45 μm).

Table I reveals that r_{in} is large, and by Eq. (2), $r_{in} = r_c + r_g + R_s$ should be minimized, i.e., L should decrease without an attendant increase in r_{in}. The value of r_{in} obtained from the y-parameter measurement is

TABLE I

COMPILATION OF DEVICE RESULTS

Run	Design	Device	Mag at 8 GHz(dB)	NF_m at 8 GHz(dB)	G_a at 8 GHz(dB)	L (μm)	r_{in} (ohms)	R_s (ohms)	V_p (V)	NF_m calc (dB)	V_s (10^7 cm/sec)
EB8	Z=150μm	8-1	14.6	5	9.5	0.63		10			
		8-2					20.6	6-10			
		8-3					39	6-10			
		8-4					29.7	∿3			
		8-5					29.7	∿3			
		8-6					36	6-10			
		8-7	16.6	4.9(V_g=0, leaky gate, wouldn't pinch off)	12.1	0.58					
		8-8					29	∿3			
EB11	Z=150μm	11-3		1.83	11	0.17	43.3	3.2	2.9	1.5	
EB13	Z=150μm	13-1	14.8	1.71	12.8	0.25			3.1		
EB16	Z=150μm	16-1	14.8	1.55	13.8	0.24			2.08	1.49	1.47
		16-2	17.1	1.47	15.7	0.167		7.75	1.34		1.45
		16-3	18.8	1.45	14.3	0.182		6.8	1.25		1.32
		16-4				0.25	24.4	9.4			
		16-5				0.19	41.8				
		16-6				0.16	30.3				
EB18	Z=150μm	18-1		1.7	11.5	0.27			3.3		
		18-2		2.37	12.9						
EB19	Z-75μm		15-16								
		19-2				0.55	15.1		2.1	1.6	
		19-3		2.13	11.3	0.36		9.7			
		19-4	16 at 12 GHz								
		19-5		2.4	10.6						
EB20	Z=75μm	20-1		1.96	15.7						
		20-2		2.14	13.9	∿0.35*					
EB21	Z=150μm	21-1	16	3.11	13.8						
	Dual Pad	21-2	18.8	1.92	14	∿0.4*					
		21-5					14.1		2.2		
		21-6	18.4	1.68	14.2	∿0.4*					

* Rough optical measurement

$$r_{in} = \frac{g_{11}}{g_m^2 + (b_{11} - \omega C_{gd})^2} = r_c + r_g + R_s + \frac{g_m L_s}{C_{gs}} \qquad (3)$$

where C_{gs} is the gate capacitance and L_s is the source inductance. Table I reveals that R_s does not dominate r_{in} Table II reveals that r_c does not dominate r_{in} either, since one would expect r_c to increase several times over in going from a gate bias of zero to near pinch-off V_p, and yet r_{in} changes very little.

TABLE II

The Effect of r_c on r_{in}

Device	r_{in} (V_g=0) (ohms)	r_{in} (V_g near V_p) (ohms)	V_p (V)
EB6-1	18.2	20 at V_g = -2V	3.5
EB6-5	28.6	29.5 at V_g = -1.7V	2.8
EB11-3	43.3	45.7 at V_g = -1.77V	2.9

Concerning $g_m L_s/C_{gs}$, Table III reveals that r_g is the dominant factor in determining r_{in} (Table II suggests that r_c can be ignored).

Section 4 deals with the problem as to why r_g is so high and relates the efforts made to reduce it apart from a change in the device geometry. Runs EB19 and EB20 used the same geometry as the previous runs, with the exception that the device width was halved to 75 μm while Run EB21 main-

TABLE III

Determination of r_g from r_{in}

Device	L (μm)	r_{in} (ohms)	R_s (ohms)	$\frac{g_m L_s}{C_{gs}}$ (ohms)	$r_g = r_{in} - R_s - \frac{g_m L_s}{C_{gs}}$ (ohms)
EB16-4	0.25	24.4	9.4	6.85	8.2
EB16-5	0.19	41.8	10.0*	7.55	24.3
EB16-6	0.16	30.3	7.0*	7.65	15.7

*Not directly measured, but computed as the worst-case upper limit.

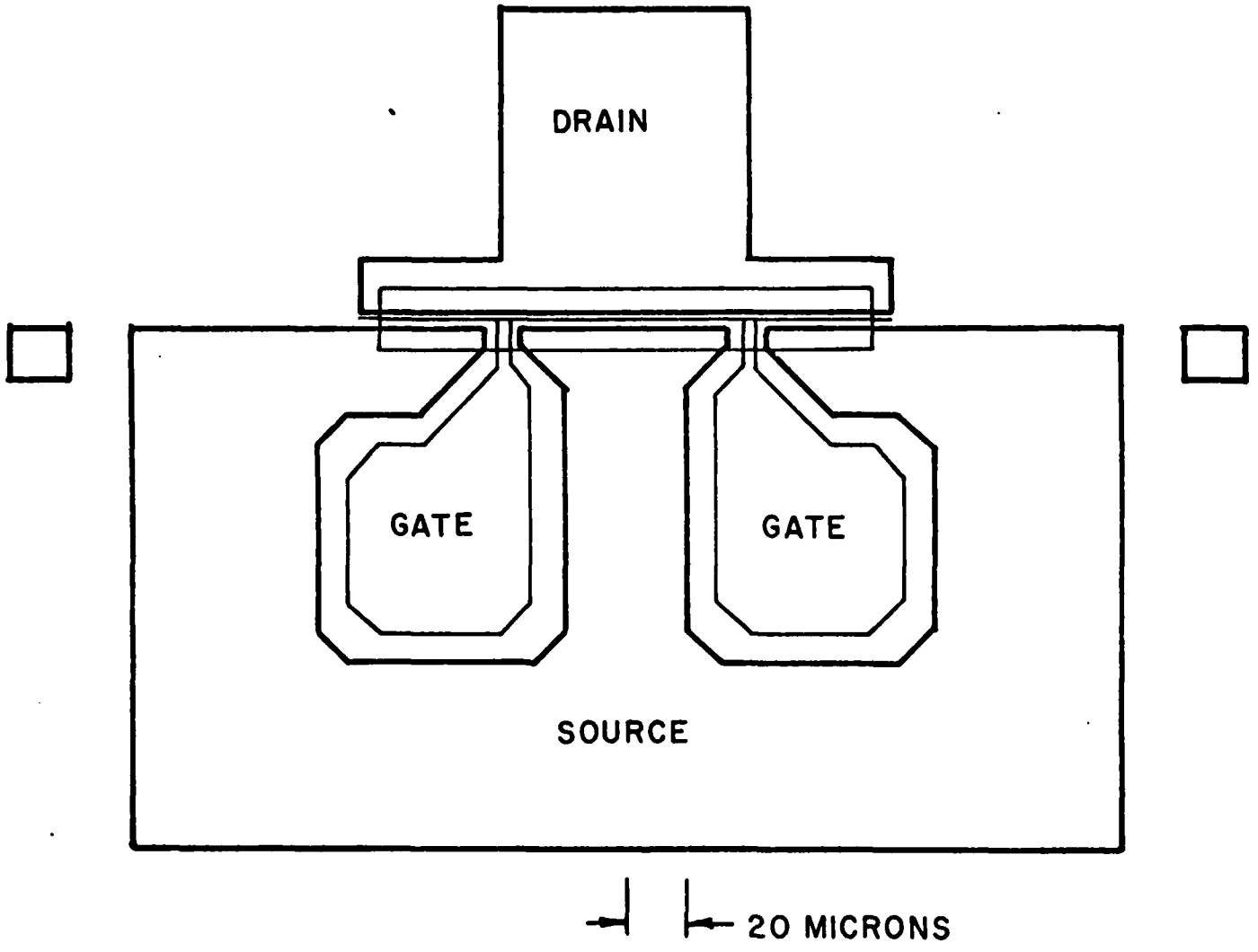


Fig. 5 Dual gate pad geometry.

tained the 150-μm width and resorted to two gate pads to reduce the gate resistance (Fig. 5). Table I indicates the success of runs EB19 to 21 is lowering r_{in}, but to date lower noise figures have not resulted, primarily because of the longer gate lengths (the result of using a new mask set and using a new computer with its different writing speed -- see Sec. 3 for details).

Run EB16 was used to determine the breakdown of R_s into its components -- R_c, R_{n+} and R_n -- as defined by Fig. 6.

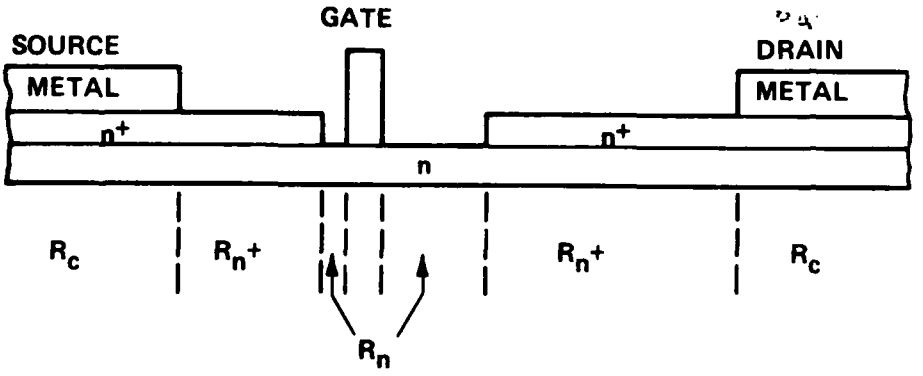


Fig. 6 Source resistance breakdown into component values.

For the three devices for which R_s and the drain resistance R_d were measured (EB16-2, 3 and 4), assuming R_c and the per-unit-length values of R_{n+} and R_n were the same for each device, a set of simultaneous equations were solved to determine these values. The number of unknowns was less than the number of equations and it turned out that it was impossible to derive solutions that would satisfy all the equations (which would mean that the initial assumption that these values were the same for all the devices was in error), but roughly for Run EB16, the breakdown is:

$$R_c \cong 1.5 \text{ ohms}$$

$$R_{n+} \cong 3\text{-}4 \text{ ohms}$$

$$R_n \cong 3 \text{ ohms}$$

This shows that the gate-metallization spacing ($R_{n+} + R_n$) dominates over the contact resistance portion. However, assuming $\rho_c = 10^{-6}\text{ohm-cm}^2$, $N_D = 2.5 \times 10^{18}\text{cm}^{-3}$ and 1000 Å for the n^+ layer, and $3.5 \times 10^{17}\text{cm}^{-3}$ and 700 Å for the n layer, theoretically

$$R_c = 0.747 \text{ ohm}$$

$$R_{n+} = 0.833 \text{ ohm}$$

$$R_n = 0.48 \text{ ohm}$$

assuming bulk mobilities. Thus, R_s should be more like 2 ohms rather than the 7-9 ohms actually measured.

One of the reasons why R_s has not been explored further is because SEM observation of the channel region is needed to obtain the various spacings, and this invariably degrades

the device. Although the form of the drain characteristic remains the same, I_{dss} is reduced to ~2/3 of its original value when observed with the SEM. The gate leakage remains the same, and the only noticeable changes that are apparent can be described as a decrease in the channel saturated velocity and mobility.

3. DETAILED CHRONOLOGICAL DESCRIPTION OF PROGRESS

3.1 Runs EB7 to EB11

All the runs used n^+ on n MBE material with the n^+ layer nominally 1000 Å thick and doped $3.5 \times 10^{17} cm^{-3}$. The practice of anodically removing the n^+ layer in the gate regions while protecting the ohmic contacts with a W-Ti/SiO_2 combination was continued. Figure 4 gives the processing sequence.

It had appeared from run EB6 that the noise performance was limited by a high resistance interface layer between the gate metallization and the GaAs. To circumvent this, runs EB7-EB9 were given an HF rather than an HCl etch to strip off the final anode oxide growth and were also given a pre-bake in vacuum before the gate metal deposition to drive off any remaining water (the very small resist openings may retain moisture). For runs EB10 and EB11, the final anodic oxide growth was removed and followed with a plasma etch using CF_4 in an effort to reduce the surface residue even further.

Of these five runs, only EB8 and EB11 gave completed devices. The main problem with all of these runs is the poor adherence of the SiO_2 to the W-Ti, causing destruction of the ohmic contacts while anodizing. Several of the runs had considerable delay between the deposition of the W-Ti and the deposition of the SiO_2 because of equipment scheduling problems, compounding the problem even further. A few devices managed to escape intact for runs EB8 and EB11. For the good devices of run EB8, uneven anodization prevented pinchoff so that the optimum bias for minimum noise figure

NF_m could not be obtained. Table I summarizes the rf data obtained in an amplifier circuit at 8 GHz.

It was quite clear at this point that something must be done to remedy the anodization damage. Clearly the SiO_2 adhesion to the W-Ti is marginal even when put down immediately after the W-Ti deposition.

3.2 Runs EB12 to EB15

As previously, all the runs used n^+ on n MBE material with the n^+ layer nominally 1000 Å thick and doped 3.5×10^{17} cm^{-3}. The practice of anodically removing the n^+ layer in the gate regions was continued, with a final plasma etch using CF_4.

Run EB12 was a dummy run to evaluate the merits of using Al over the W-Ti in order to improve the SiO_2 adhesion, and for this run there was a large decrease in the amount of damage incurred during anodization. Run EB13 (MBE wafer #124) was completed using Al over the W-Ti; but for some reason the anodization damage was much worse than for EB12 and only one device was tested with the results shown in Table I. In trying to rebond the device in an s-parameter jig, the device was destroyed due to the ohmic contact metallization pulling off with the bonds. No devices were obtained from runs EB14 and EB15 because of poor resist lithography (the resist may have been too old) and thermal overshoot in the CVD reactor, respectively.

3.3 Runs EB16 to EB18

The yield for run EB16 (MBE wafer #126) was relatively

high for the anodic thinning, giving plenty of devices for testing. Most of the devices had quite low currents (10 mA or less), indicating the MBE active layer was thinner or lower doped than previously. Either the anodization was different or the n^+ and/or the active layers were thinner. Three devices were rf tested at 8 GHz and the results are shown in Table I. These were by far the best results obtained so far, and were the best results obtained for MBE material as reported in the literature to date. According to Liechti's article in the October 1978 issue of Microwaves,[6] the noise figure is about state-of-the-art for 0.5-micron gate lengths, but the associated gain is much higher, being even higher than that projected for 0.25-micron devices. The uncertainty in the noise measurement is around ±0.6 dB (e.g., the solid-state noise diode itself is calibrated only to within ±0.3 dB at 8 GHz).

Noise measurements were made on the same devices using a hot-cold noise source. This measurement should be more accurate than with the solid-state diode noise source used previously; however, the results were comparable to the previous results. A device from run EB16 was bonded up in a 25-GHz amplifier circuit. A minimum noise figure of 4.7 dB and an associated gain of 3.9 dB were measured at 25 GHz.

S-parameter measurements were made on other devices from run EB16 to determine the input resistance. It is virtually impossible to unbond devices from the noise figure amplifier circuit and rebond them in the s-parameter jig. The input resistances as determined from the s-parameters are shown in Table I.

Measurement of R_s gave around 8 to 9 ohms, which was higher than the 3-ohm values obtained for previous runs, but this was primarily due to the thinner active layer. Analysis of R_s gave 1.5 ohms for the contact resistance, 3-4 ohms for the n^+ layer and 3 ohms for the n^+-gate spacing. It can be seen from Table I that the input resistance does not correlate well with the gate length (which it should if the gate resistance is assumed to dominate), making it difficult to assign a unique value of input resistance for computational purposes to the devices on which the noise figure measurements were made. With R_s and presumably the channel resistance approximately the same for each device, the variation in the input resistance should be due to the gate, and the fact that this resistance does not correlate with gate length may mean that the gate metal cross-sectional profile may vary significantly between devices.

Run EB18 was done (MBE wafer #126) with a wider gate lead out to the gate pad. Only two anodizations rather than the three done for run EB16 were done to the gate regions, resulting in high current devices. Two devices were tested at 8 GHz, with the results in Table I. It would seem that a thinner recessed channel results in lower noise figures and higher associated gains, considering that run EB16 was made on the same wafer. It is interesting that this dependence on channel thickness is not suggested by the BTL noise figure formula (Eq. (2)).

3.4 Techniques to Reduce Anodization Damage to Ohmic Contacts

A run was tried with the gate anodized and deposited

before the source-drain metallization deposition. The source-drain overlay was used for alignment, and because this pattern is set back from the channel area, no anodization damage occurred. However, as might be expected, the Au gates degraded electrically when the ohmic contacts were alloyed. This prompted the investigation of non-alloyed ohmic contacts using highly-doped MBE material.[7]

A 1000 Å thick MBE layer doped to ~$10^{19}cm^{-3}$ was grown and Au-Ge/Ni/Au contacts were deposited on it. As deposited, the contacts were ohmic with a specific contact resistance of 2-3 x $10^{4}ohm\text{-}cm^{2}$. A sinter at 300°C did little to improve this resistance, while at 350°C (about the highest that can be tolerated without damaging the gate) it reduced to 2 x $10^{-6}ohm\text{-}cm^{-2}$. If the doping can be raised to ~5 x $10^{19}cm^{-3}$, the specific contact resistance should drop below $10^{-6}ohm\text{-}cm^{2}$, enabling the gates to be anodized before the ohmic contact formation.

3.5 New Mask Set Runs

The new mask set has two FET patterns, one with two gate pads and Z (device width) = 150 microns as before (Fig. 4) and the other a half-width version of the one used previously with Z = 75 microns. The software had not been developed for the writing of the gate of the dual-gate pad device at the time the new mask set was received. In addition, the 620/i minicomputer originally used was being replaced by an LSI-11 computer. For the Z = 75 micron device, all that is needed is a change in the SEM magnification (the connection to the gate pad is not narrowed,

since its width is more a function of the number of times the beam traverses the length of the connection). Consequently, the initial effort at using the new masks was towards fabricating the Z = 75 micron wide devices.

Two trial runs were done on MBE wafer #189 with the Z = 75 micron patterns. The resist exposure was recalibrated to compensate for the smaller exposure needed for the smaller device width and also because of the altered resist profile in the channel brought on by reducing the source-drain metallization spacing from 3 to 2.4 microns. Because of the severe damage to the ohmic contacts during the anodization, the device yield was zero. After the SiO_2 deposition, a fringe developed around the ohmic contact edges which extended out into the channel and apparently was responsible for the anodic etch reaching the ohmic contacts and destroying them. This fringe was not apparent before the SiO_2 deposition and perhaps was a result of some Al-Au interaction around the edges of the W-Ti during the 350°C CVD SiO_2 deposition.

Run EB19 was done using another portion of MBE wafer #189. This wafer is the first MBE FET wafer using SnTe,[8] and in addition to this, the n^+ doping was raised from ~2.5 x $10^{18}cm^{-3}$ to ~$10^{19}cm^{-3}$ by lowering the substrate temperature to 533°C during growth. To avoid the low-yield problem with anodization, the n^+ layer was removed using a citric acid etch. The W-Ti/Al layers were not included in the ohmic contacts, thus reducing the height of the ohmic contacts and improving the resist uniformity in the channel region. The gates were intentionally overexposed since it seemed that the gate exposure was more difficult to optically detect for the trial runs, so without checking in detail the

gate exposure was increased as a conservative measure to ensure a supply of devices. As a result of all these changes, the yield was very good with the gate lengths ranging from 0.4 to 0.5 micron.

Values of MAG ranged from 15 to 16 dB at 8 GHz for the devices of run EB19, with one device giving 16 dB at 12 GHz on the Bldg. 7 network analyzer. Devices 19-1 and 19-2 were bonded up in s-parameter jigs and s-parameter data was obtained. The s-parameter data was bad for 19-1 and that for 19-2 gave 15 ohms for the input resistance. With a gate length of 0.55 micron and a pinchoff voltage of 2.1 V, 19-2 should in theory give a minimum noise figure of 1.6 dB at 8 GHz if it had been bonded up in an amplifier jig. Device 19-3 was bonded up in an amplifier circuit and gave a minimum noise figure of 2.13 dB at 8 GHz with an associated gain of 11.3 dB. The drain characteristic of 19-3 was identical to that of 19-2, but with a gate length of 0.36 micron one would expect a minimum noise figure less than the 1.6 dB computed for 19-2. The source resistance R_s was measured to be 9.7 ohms for 19-3 and with a larger value of source-gate spacing than for 19-2, it may be that R_s was larger for 19-3 (19-3 was destroyed while trying to measure R_s). In addition, as the gate length decreases, the gate length may become more triangular so that the gate resistance increases at a faster rate than L^{-1}. When an upper limit is placed on these parameters to determine the upper limit on the input resistance (which was computed to be 37 ohms), the computed minimum noise figure is still only 1.8 dB, or 0.3 dB below the measured value. A new microstrip jig is being fabricated which will enable <u>both</u> the s-parameters and the minimum noise figure to be measured on the <u>same</u> device without

redie-bonding (which usually destroys the device). This will avoid the above confusion of trying to deduce the performance of one device from the parameters of another device by making assumptions on how their differences should be handled.

Run EB20 was made on MBE wafer #190 (same growth conditions as wafer #189) using the same 75-micron gate structure but with shorter gate lengths. Difficulty with the gate liftoff resulted in a low yield. Table I gives the rf results at 8 GHz.

Run EB21 was completed using the new dual gate pad structure shown in Fig. 7 to reduce the gate resistance. Table I summarizes the rf performance obtained from this run. The gate metallization for EB21 was unintentionally thin. Difficulty in optically determining whether or not the gate exposures were good and difficulty in seeing the SiO_2 edge to determine when to cease etching plagued this run, being a product of the new mask set and using a new computer with its different writing speed.

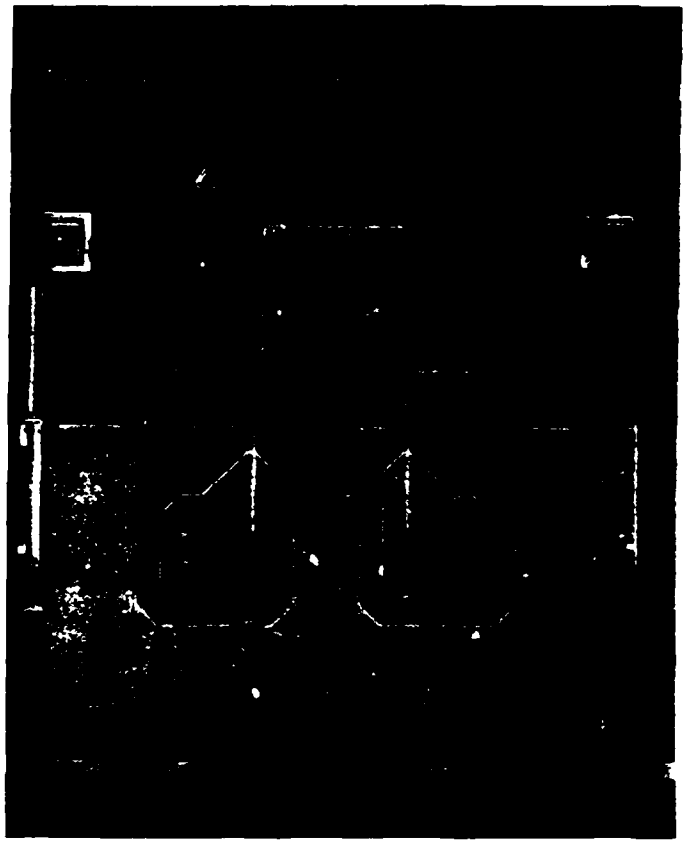


Fig. 7 Dual Gate Pad FET.

4. GATE RESISTANCE REDUCTION

As mentioned in Sec. 2, gate resistance appears to be one of the prime limitations towards improving the noise performance of the FETs. An effort was made to determine the maximum gate metal thickness that can be lifted. Al evaporations of 5200, 8100, and 8800 Å were done. Good liftoff was obtained for all three thicknesses. For the two thicker evaporations, the gates were triangular in cross-section coming to a sharp point at the top (Fig. 8), and both were about 6000 Å high with about a 0.2-micron opening in the resist. It thus appears that the resist opening is gradually closed by metal buildup on the edge of the resist mask defining the gate electrode during the deposition process. This problem appears to be basic to the fabrication of such a small gate length.[9] For this run, there was no merit in evaporating more than 6000 Å of metal. When Au was evaporated, the height of the triangle was less than when Al was used, indicating that Au builds out over the gate opening faster than Al. However, the use of Al as the gate metal results in g_m compression at zero gate bias. Whether the Au has an effectively larger source area than the Al by wetting outwardly over more of the evaporation boat, or the Au tends to stick better to a vertical edge, is not known.

Several techniques were tried in order to plate up the gate to decrease its resistance. With a negative potential on the gate and the epitaxial layer floating, Au was found to plate in the channel area. Realigning the resist to the gate pattern gave mushroom gates, but not only was realign-

Fig. 8 Triangular gate shape.

ment very difficult (as can be imagined) but it appeared that the plating solution attacked the resist-GaAs interface slightly, causing Au to plate under the resist edge and to thereby lengthen the gate (Fig. 9). Postbaking the resist did not solve this latter problem.

A bias was also applied to the epitaxial layer to prevent plating on it. With a positive bias on the epitaxial layer, the GaAs apparently acts like an anode with respect to the gate and etches in the regions adjacent to the gate and perhaps plates Ga onto the gate. There does not appear to be any threshold voltage below which this does not occur to some degree. The end result was a perfectly round gate with adjacent etched troughs in the GaAs (Fig. 10).

Another technique that was tried was to spin on new resist after the gate liftoff and then thin it with MIBK until the tips of the gates are exposed. The exposed tips are then plated up into a mushroom structure (Fig. 11). The problem with this technique is getting the gate metal high enough (typically higher than the ohmic contact height) so that the resist to be thinned is a bump rather than in a dimpled region between the source and the drain where, by the time enough resist is removed to expose the top of the gate, not enough remains to prevent plating in the channel region. Although it is quite easy to achieve sufficient height using Al, the use of Au results in a lower height triangle for the same resist opening. Besides not being able to tell when the tips of the gates were exposed through the resist in order to be able to plate them, a resist postbake did not prevent Au from plating in the channel regions adjacent to

Fig. 9 Mushroom gate illustrating misalignment and plating under the resist.

Fig. 10 Plated gate with active layer bias, showing etched GaAs.

Fig. 11 Mushroom gate using resist thinning.

the gate edge and thereby lengthen the gate. It may be that the resist thinning process or the plating process causes the resist to pull away from the gate metal and hence widen the gate. Although the possibility exists that this technique could be made to work (perhaps a Ti layer would improve the adherence of the resist to the Au gate), arrival of the new mask set of Fig. 5 to lower the gate resistance shifted the emphasis away from using plating techniques to lower the gate resistance.

Table I demonstrates the lower values of r_{in} resulting from the new mask set. Table IV deduces r_g from r_{in} for run EB19, revealing lower values of r_g than for the corresponding run EB16 tabulation in Table III. The longer gate lengths in Table IV would of themselves result in lower values of r_g, all other things remaining equal. With Z reduced to half its value, one would expect r_g to drop a factor of two.

TABLE IV

Gate Resistance of Run EB19

Device	L (micron)	r_{in} (ohms)	R_s (ohms)	$\frac{g_m L_s}{C_{gs}}$ (ohms)	$r_g = r_{in} - R_s - \frac{g_m L_s}{C_{gs}}$ (ohms)
19-2	0.55	15.1	6.3-9.7	3.2	2.2 - 5.6
19-5	0.34	18.1	7.2	4.0	6.9

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

During this period, the rf performance at 8 GHz was improved from a minimum noise figure of 2.2 dB with an associated gain of 12 dB to a minimum noise figure of 1.5 dB with an associated gain of 15 dB. These results are the best obtained for MBE material as reported in the literature to date. This was primarily accomplished by a reduction in gate length. The parameter limiting device performance is primarily the gate resistance, which is high because of the resist opening being gradually closed by metal buildup on the resist edge during the evaporation. Efforts to plate up the gate were not successful, and a new mask design to lower the gate resistance has been implemented, but to date improved performance has not been realized because of the longer gate lengths (the result of using a new mask set and using a new computer with its different writing speed). Also, R_s appeared to be significantly higher than it should be from theoretical considerations by about a factor of 3 or 4.

The problem with anodization damage was eliminated by going to a citric acid etch in the gate region in place of the anodic etching. The uncertainty in the exact doping profile of the MBE layers has been dealt with by monitoring the channel current as the gate region is thinned. It appears that better noise figures result when the active layer is thinned below its 1200 Å as-grown thickness, thereby diminishing the importance of stopping the thinning abruptly at the n^+-n interface.

Future work should concentrate on reducing the gate length with the new mask set. Once r_g falls below R_s, R_s should be more thoroughly investigated as to why it is not as low as it theoretically should be. As to the term $g_m L_s/C_{gs}$ that is a part of r_{in}, it is not certain if this term should be included when computing the minimum noise figure. So far it has been, and it can only be reduced by reducing L_s. Figure 12 shows a geometry that might be used to reduce L_s through the use of plated-through source contacts from the back side. Figure 12 also shows how a further reduction in gate resistance can be made through the use of multiple gate connections. Once r_g and R_s have been sufficiently reduced to allow study of the properties of the intrinsic device, the ultimate goals, as listed in the Introduction, can be addressed.

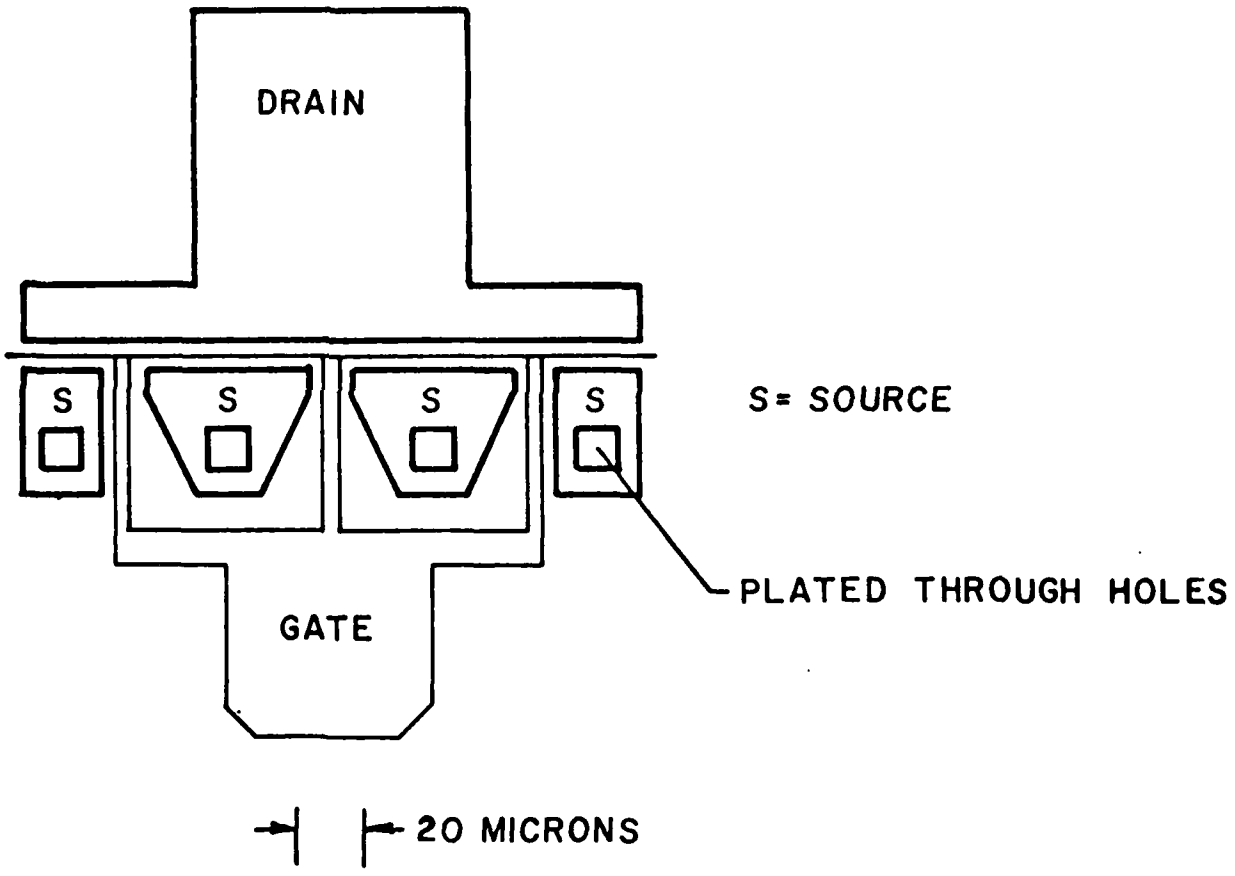


Fig. 12 Plated through source geometry.

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